

S/N Unknown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wendell P. Noble Jr.	Examiner:	Unknown
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	Herewith	Docket:	303.257US4
Title:	METHOD FOR FORMING GATE SEGMENTS FOR AN INTEGRATED CIRCUIT		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Pursuant to 37 C.F.R. §1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicant's prior U.S. application, Serial No. 09/911688, filed on July 24, 2001, which is relied upon for an earlier filing date under 35 U.S.C. §120.

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Page 2

Dkt: 303.257US4

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

WENDELL P. NOBLE JR.

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2157

Date 19 September 2003 By David R. Cochran
David R. Cochran
Reg. No. 46,632

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Date of Deposit: September 19, 2003

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	Even Date Herewith
First Named Inventor	Noble Jr., Wendell
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 1 of 1

Attorney Docket No: 303.257US4

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-4,604,162	08/05/1986	Sobczak, Zbigniew P.	156	657	12/23/1985
	US-5,976,930	11/02/1999	Noble, W.P.			
	US-5,214,603	05/25/1993	Dhong, , et al.	365	207	08/05/1991
	US-5,391,911	02/21/1995	Beyer, K. D., et al.	257	522	04/22/1994
	US-5,459,341	10/01/1995	Shono, , et al.	257	208	
	US-5,539,229	07/23/1996	Noble, W.P., et al.	257	301	12/28/1994
	US-5,640,034	06/17/1997	Malhi, S.	257	341	05/18/1992
	US-5,677,867	10/14/1997	Hazani, E.	365	185	06/30/1995
	US-5,726,463	03/10/1998	Brown, D. , et al.	257	77	08/07/1992
	US-6,025,224	02/15/2000	Gall, M. , et al.	438	243	03/31/1997
	US-6,190,960	02/20/2001	Noble, W. P.	438	253	04/25/1997

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
	EP-0720221	07/03/1996	Noble, Wendell P.	H01L	21/824 2	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BAKEMAN, P. , et al., "A High Performance 16-Mb DRAM Technology", <u>1990 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, Hawaii, (June 4-7, 1990), 11-12	
		DAVARI, B. , et al., "A Variable-Size Shallow Trench Isolation (STI) Technology with Diffused Sidewall Doping for Submicron CMOS", <u>iedm Technical Digest</u> , International Electron Devices Meeting, San Francisco, CA, (Dec. 11-14, 1988), 92-95	
		KOHYAMA, Y. , et al., "Buried Bit-Line Cell for 64MB DRAMs", <u>1990 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, (June 4-7, 1990), 17-18	
		KUGE, S. , et al., "SOI-DRAM Circuit Technologies for Low Power High Speed Multigiga Scale Memories", <u>IEEE Journal of Solid-State Circuits</u> , 31(4), (April 1996), pp. 586-591	
		SUMA, K. , et al., "An SOI-DRAM with Wide Operating Voltage Range by CMOS/SIMOX Technology", <u>IEEE Journal of Solid-State Circuits</u> , 29(11), (November 1994), pp. 1323-1329	

EXAMINER**DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached